Winbond
Bus Termination Regulator
With
Over Temp. & Current Limit Protection
W83310S
W83310SG

W83310S

Datasheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1.		Oct./03	0.5	N.A.	All versions before 0.5 are for internal use only.
2.	3,9	Oct./03	0.51	N.A.	AC spec. and typical waveform update.
3	12	Feb./04	0.60	N.A.	Add the thermal data.
4	3	Jul./04	0.61	N.A.	Add min./typ. value of VIN.
5	2,3,11	Jan./06	0.7	N.A	Modify application circuit, AC characteristic and add Pb-free part no: W83310SG.
6	13	Oct./06	1.0	N.A	Update ordering information and official release of version 1.0

Table of Contents-

1. GENERAL DESCRIPTION

The W83310S is a linear regulator which provides achieves continuous 1.8 Amp bi-directional sinking and driving capability for DDR SDRAM bus terminator application. The chip simply implement a stable power supply which can track half of input power dynamically for bus terminator with a single chip; that is the chip integrates two power MOSFETs. There is no any external power device needed. The W83310S is promoted with SOP-8 power package. With W83310S design, a high integration, high performance, and cost-effective solution is promoted.

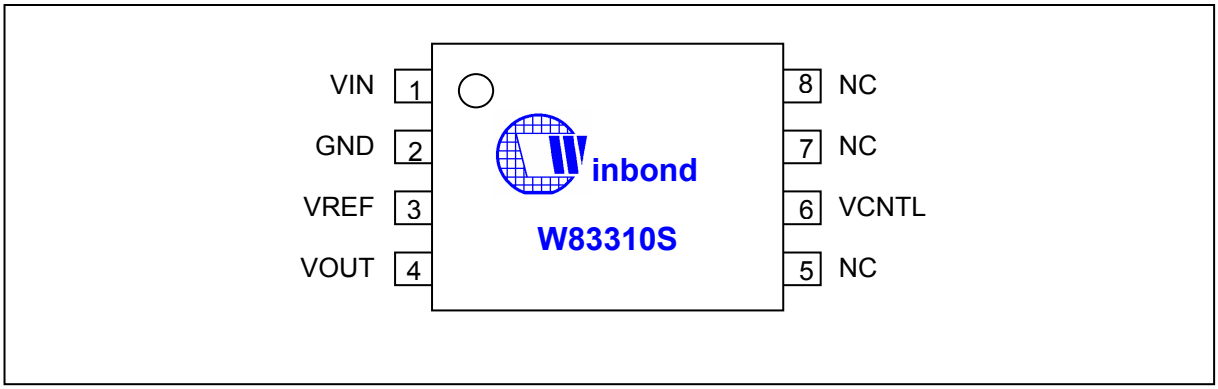
2. FEATURES

- Regulates a bi-directional power with driving and sinking capability
- Provides achieve continuous 1.8Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- Operates with +3.3V and +2.5V control power
- Current limit protection
- Over temperature protection
- Power package SOP-8
- Low cost and easy to use

3. APPLICATIONS

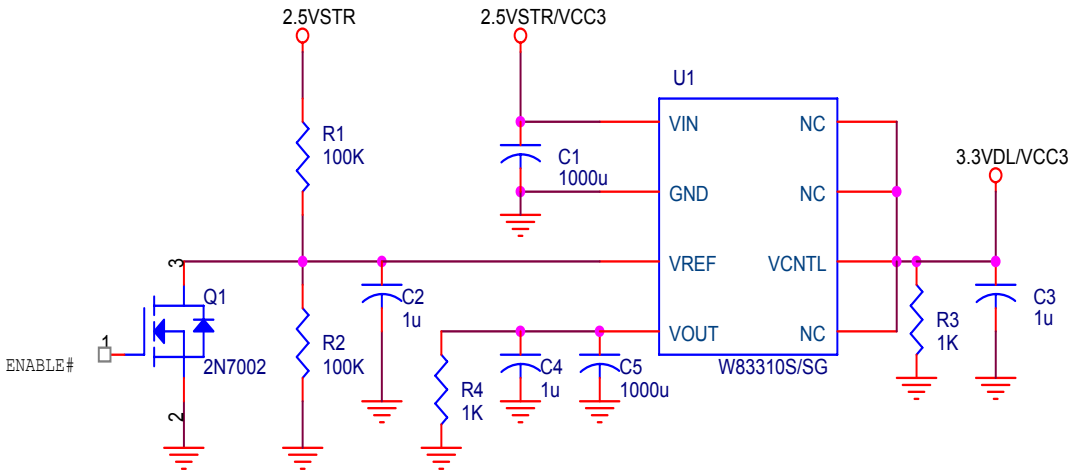
- DDR and DDR II Bus Termination Regulator
- Active Termination Bus
- SSTL-2
- SSTL-3

4. PIN CONFIGURATION AND DESCRIPTION



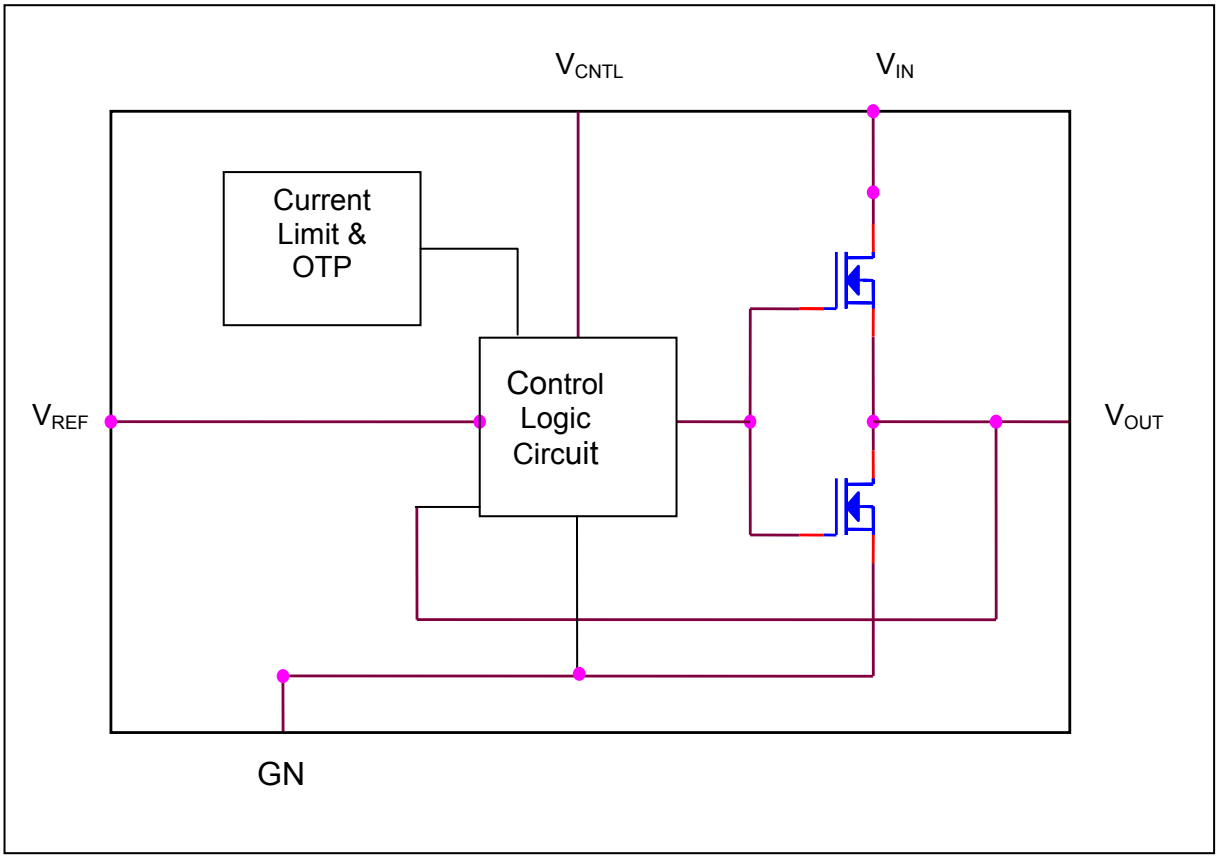
SYMBOL	PIN	FUNCTION
VIN	1	Power input pin.
GND	2	Ground.
VREF	3	Reference voltage and Chip enable.
VOUT	4	Output voltage.
NC	5	No function
VCNTL	6	Gate drive voltage.
NC	7	No function
NC	8	No function

5. APPLICATION CIRCUIT



Note:
R4=1 Kohm reserve for VOUT discharge or sink internal bias when VIN is not present but VCNTL is present.
R3=1 Kohm reserve for sink internal bias when VCNTL is not present but VIN is present.

6. INTERNAL BLOCK DIAGRAM- W83310S



7. ELECTRICAL CHARACTERISTICS

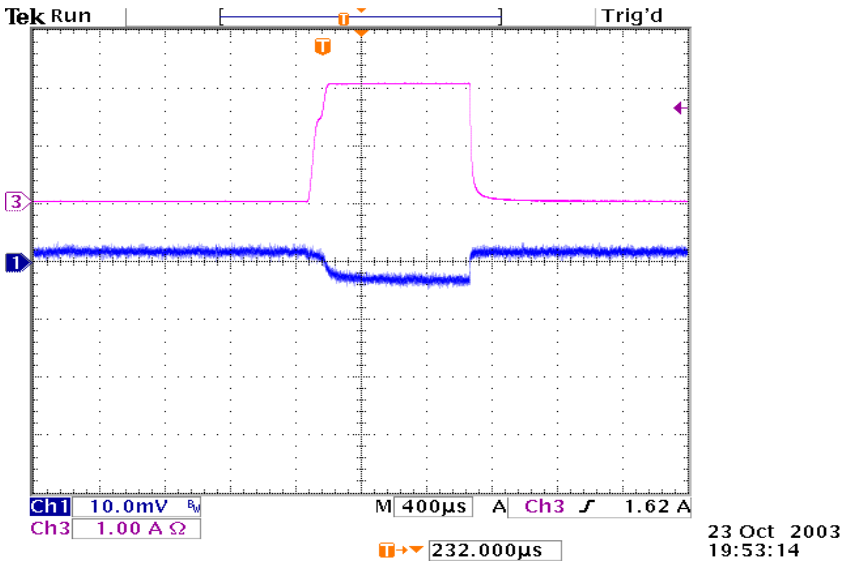
7.1 AC CHARACTERISTICS

W83310S						
VIN=2.5V,VCNTL=3.3V,VREF=1.25V,COUT=100UF, T_A = 0℃ TO +70℃						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Output Offset Voltage	V_{OS}	-20		20	mV	I_{OUT}=0A
Load Regulation		-20		20	mV	Loading: 0A→2.0A
		-20		20		Loading: 0A→-2.0A
Input Voltage Range	V_{IN}	1.7	2.5/1.8	3.63	V	
	V_{CNTL}		3.3	3.63		
Operating Current of VCNTL	I_{VCNTL}		1	1.5	mA	No Load(I_{OUT}=0A)
Operating Current of VIN	I_{VIN}			1	mA	No Load(I_{OUT}=0A)
Shutdown Threshold Trigger		0.8			V	Output=High
				0.2	V	Output=Low
Shutdown Current of VIN	I_{SHDN}		50		uA	VREF<0.2V Loading=50 mA
Short Current Limit	I_{LMT}	4			A	Output short to GND
Over Temperature Protection	**OTP**	130	145		℃	

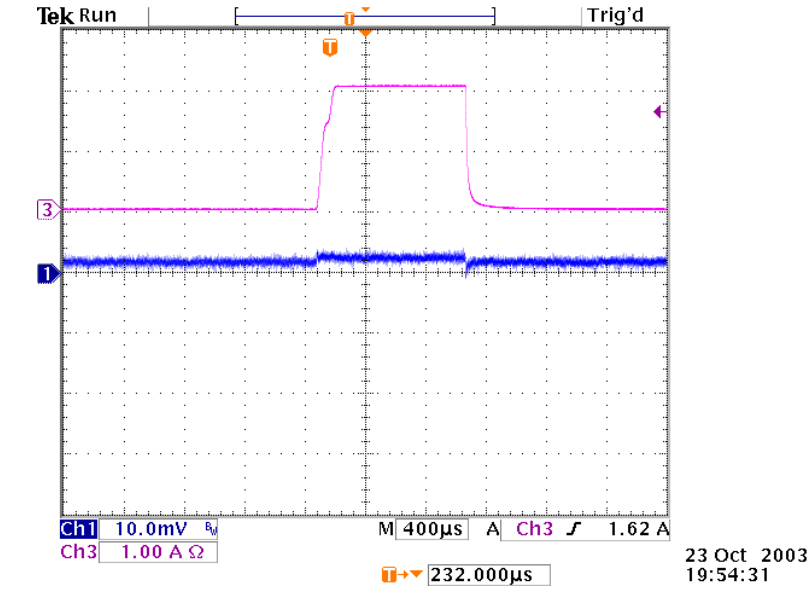
Note: Load regulation is tested with a 1ms duty pulse current and measuring V_{OUT}.

8. TYPICAL OPERATING WAVEFORM

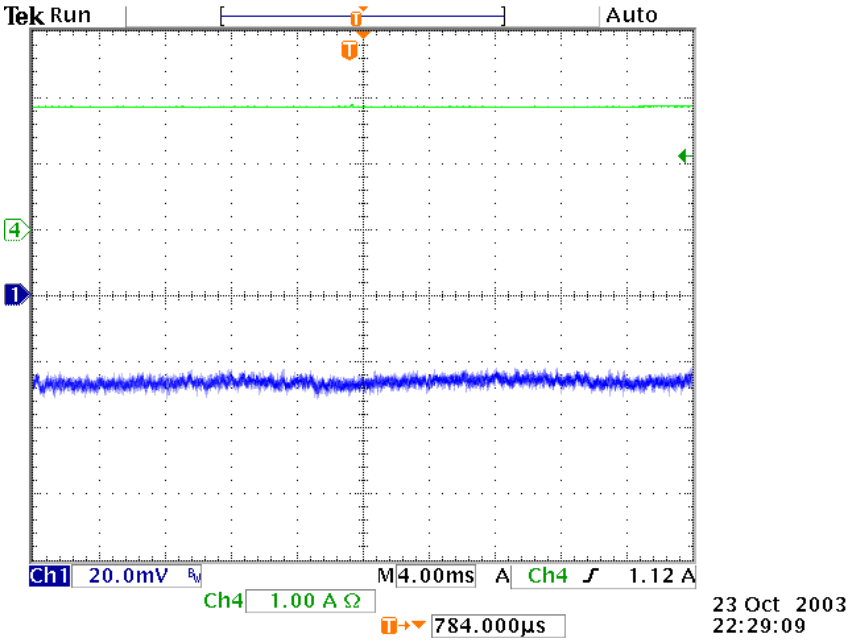
-- Load regulation with test condition - V_{CTRL}=3.3V; V_{IN}=2.5V; V_{OUT}=1.25V; 2.0Amp 1ms duty pulse driving current. $\Delta V \approx 6mV$.



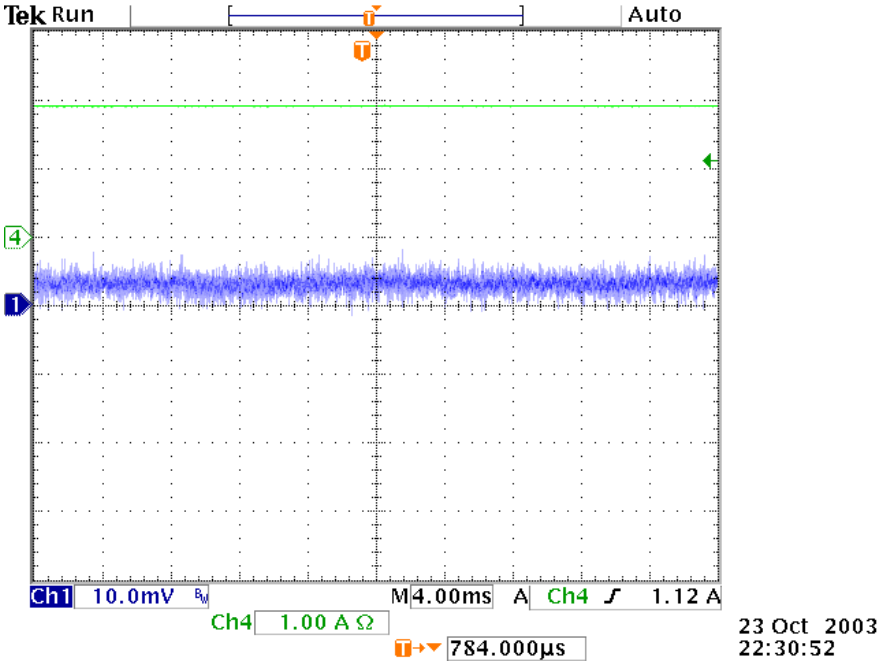
-- Load regulation with test condition - V_{CTRL}=3.3V; V_{IN}=2.5V; V_{OUT}=1.25V; 2.0Amp 1ms duty pulse sinking current. $\Delta V \approx 2mV$.



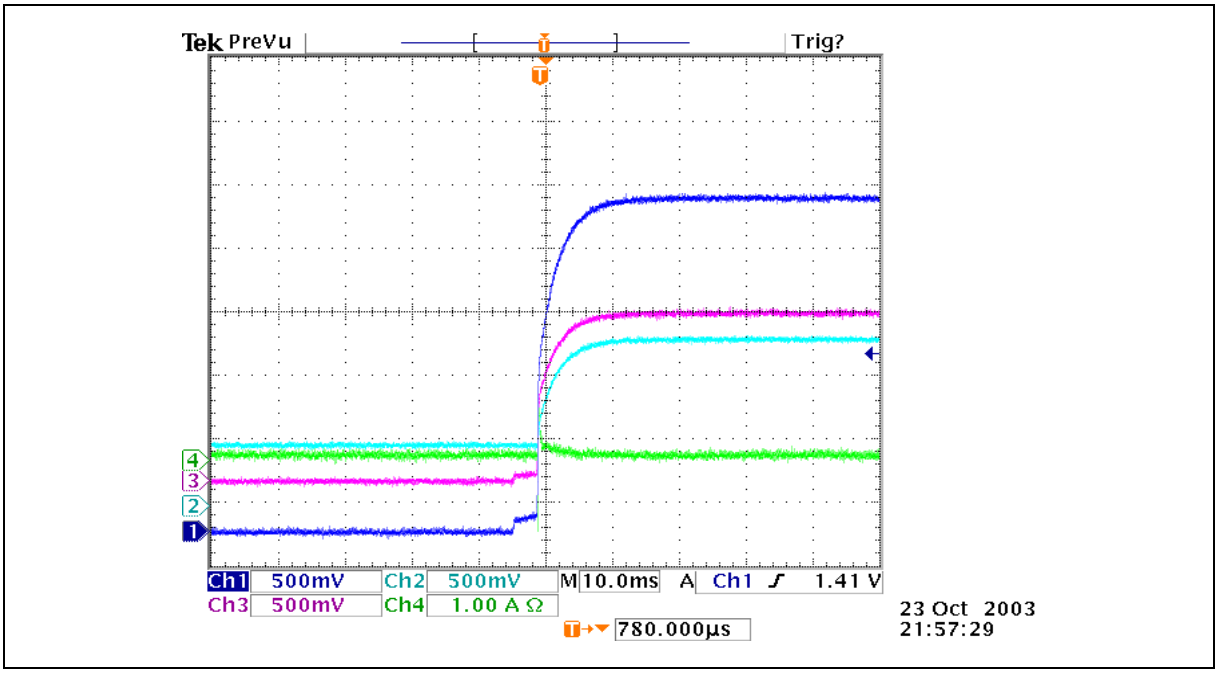
-- Load regulation with test condition - V_{CTRL}=3.3V; V_{IN}=2.5V; V_{OUT}=1.25V; 1.8Amp cont. driving current. $\Delta V \approx 24mV$.



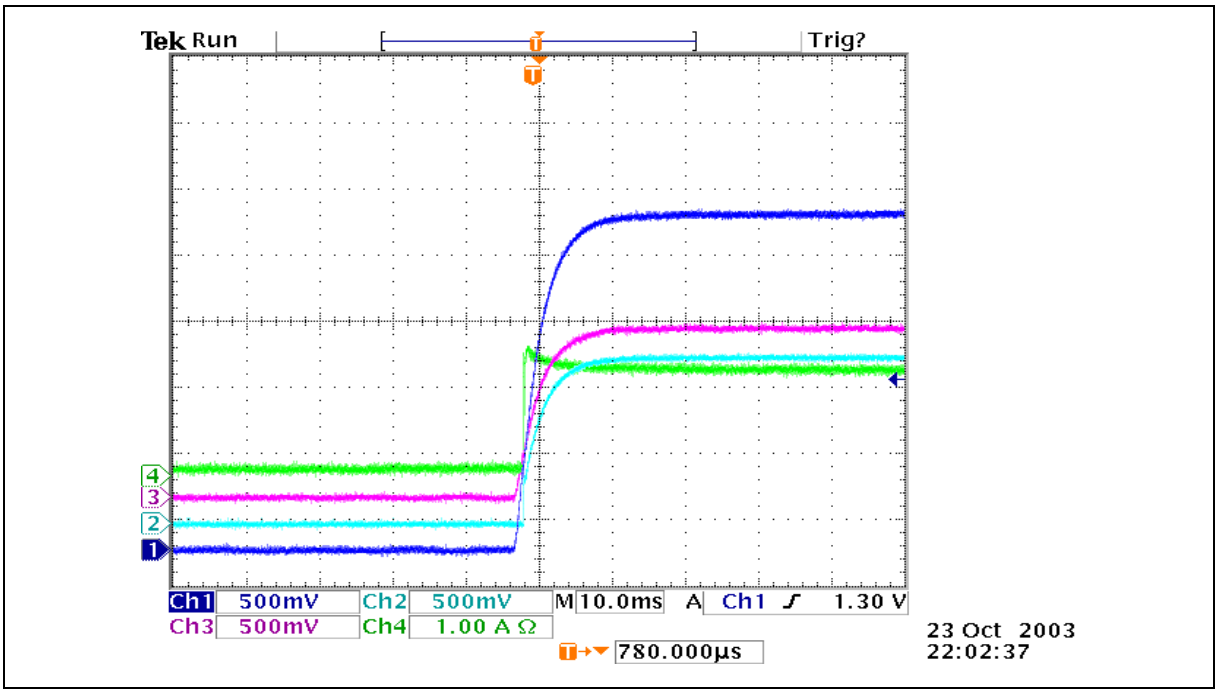
-- Load regulation with test condition - V_{CTRL}=3.3V; V_{IN}=2.5V; V_{OUT}=1.25V; 1.8Amp cont. sinking current. $\Delta V \approx 5mV$



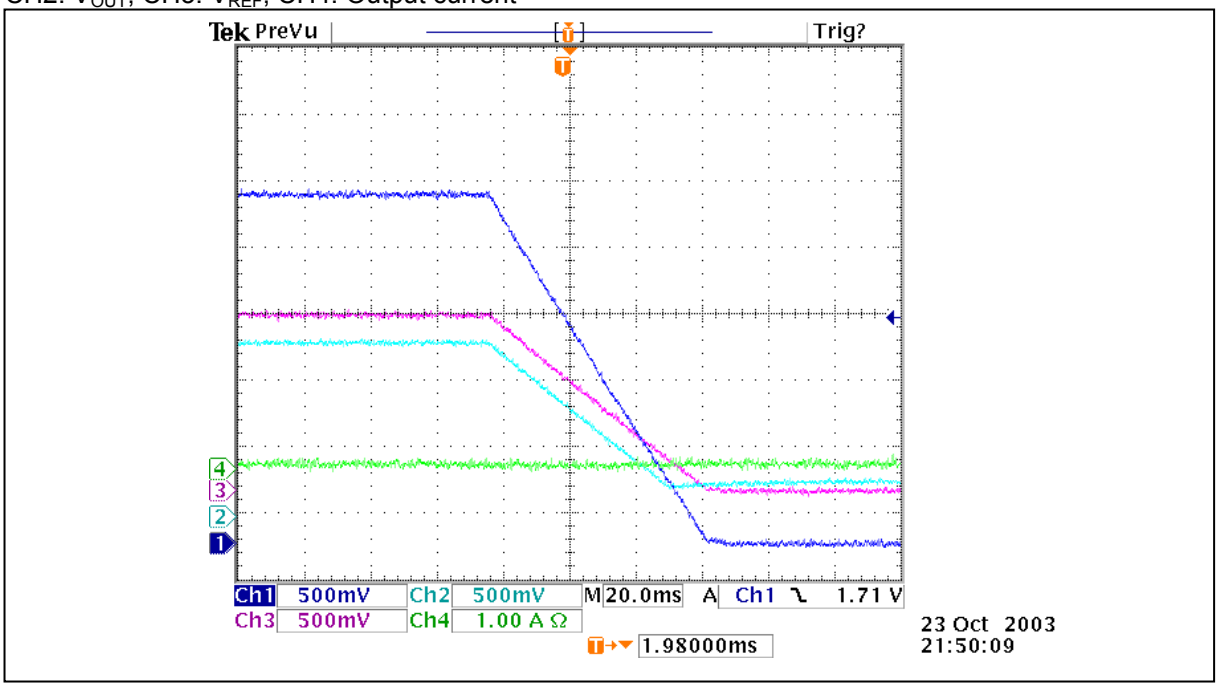
-- Power on waveform with condition: DC loading 0A; V_{IN} Cap.: 1000uF; V_{OUT} Cap.: 1000uF. CH1: V_{IN}; CH2: V_{OUT}; CH3: V_{REF}; CH4: Output current



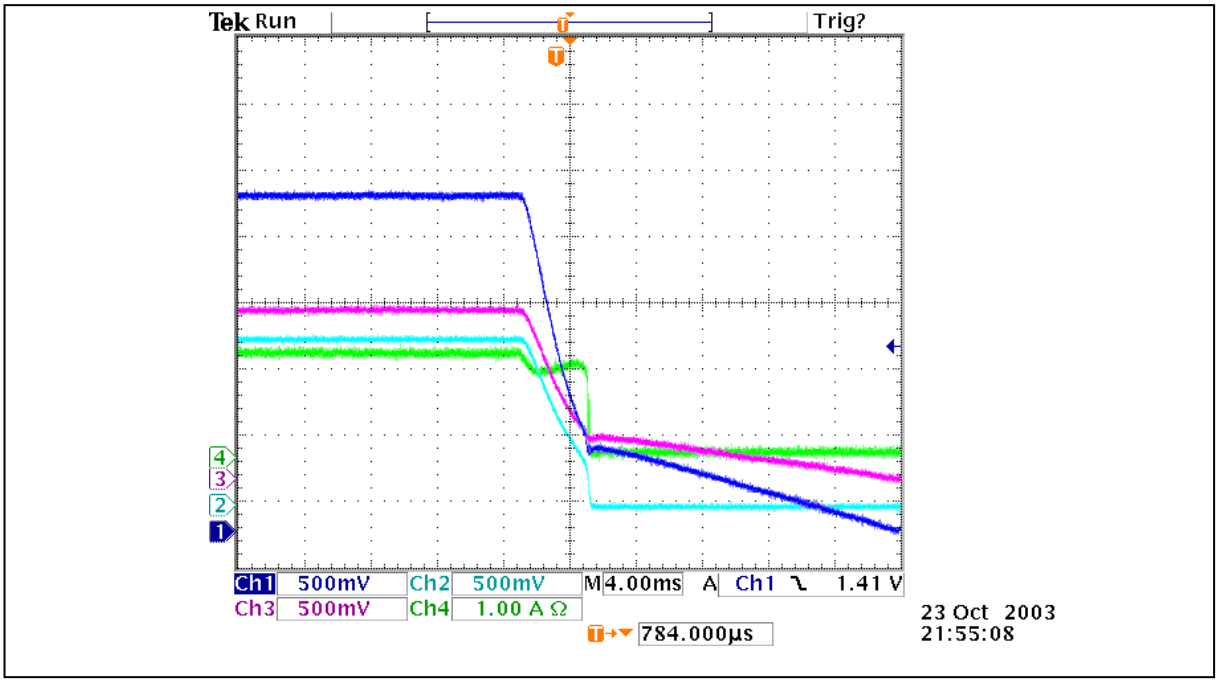
-- Power on waveform with condition: DC loading 1.5Amp; V_{IN} Cap.: 1000uF; V_{OUT} Cap.: 1000uF. CH1: V_{IN}; CH2: V_{OUT}; CH3: V_{REF}; CH4: Output current



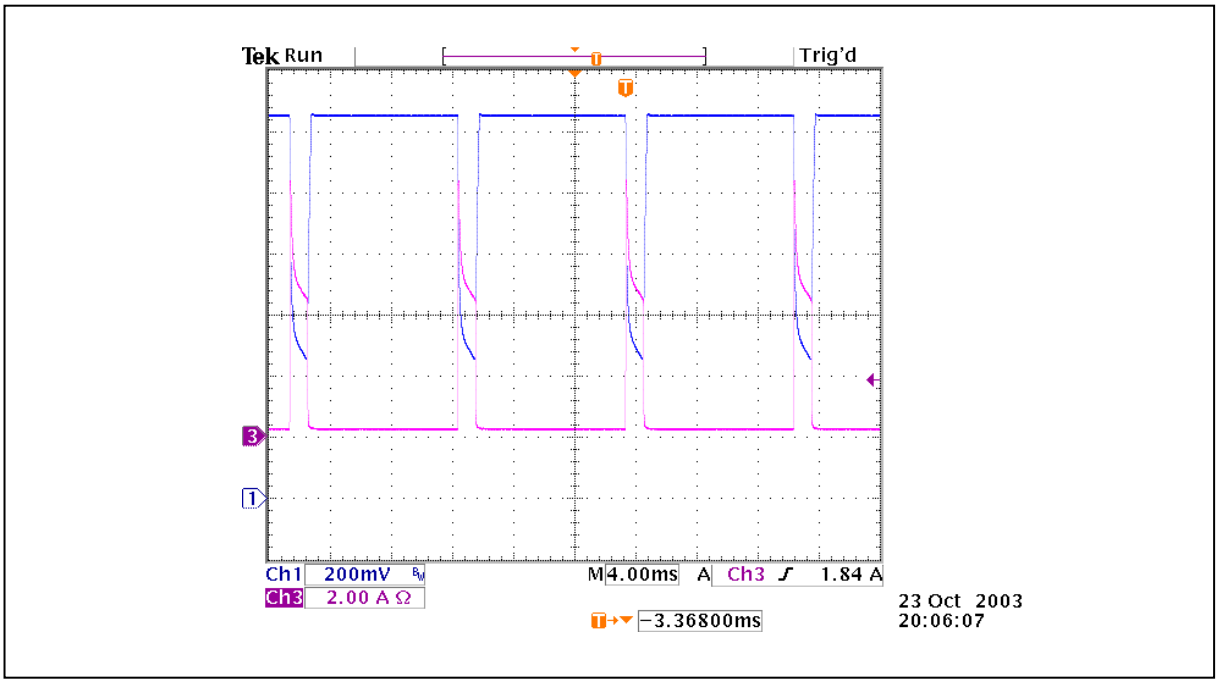
-- Power off waveform with condition: DC loading 0A; V_{IN} Cap.: 1000uF; V_{OUT} Cap.: 1000uF. CH1: V_{IN}; CH2: V_{OUT}; CH3: V_{REF}; CH4: Output current



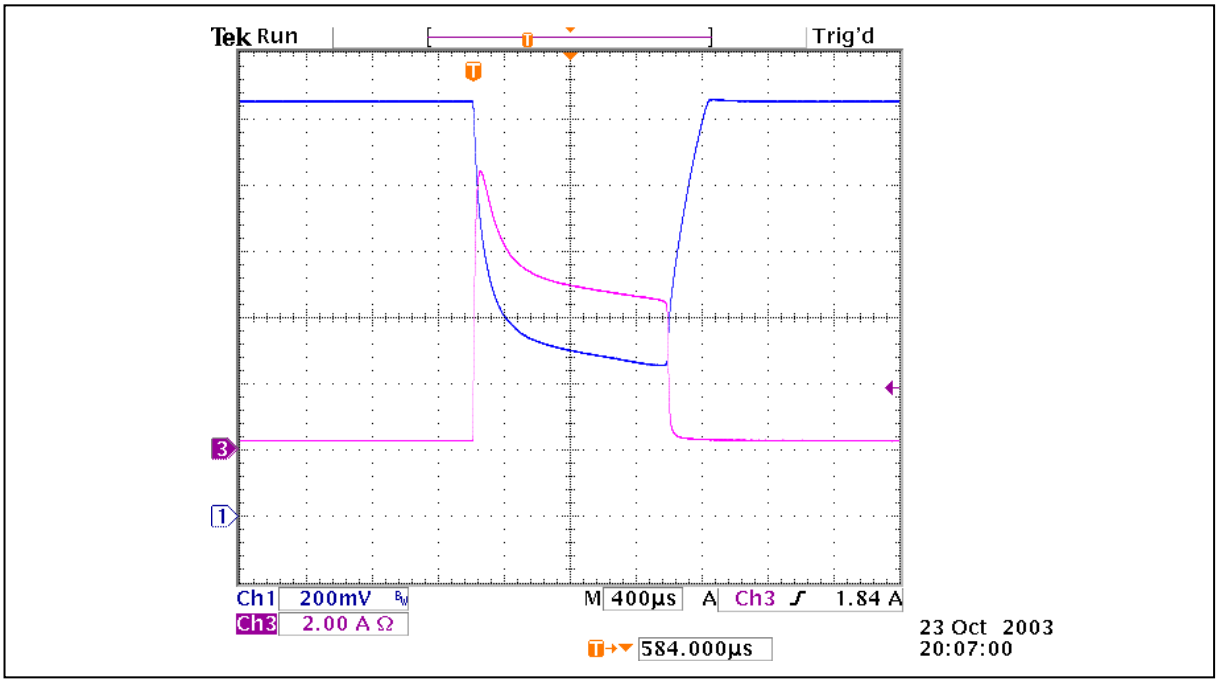
-- Power off waveform with condition: DC loading 1.5A; V_{IN} Cap.: 1000uF; V_{OUT} Cap.: 1000uF. CH1: V_{IN}; CH2: V_{OUT}; CH3: V_{REF}; CH4: Output current



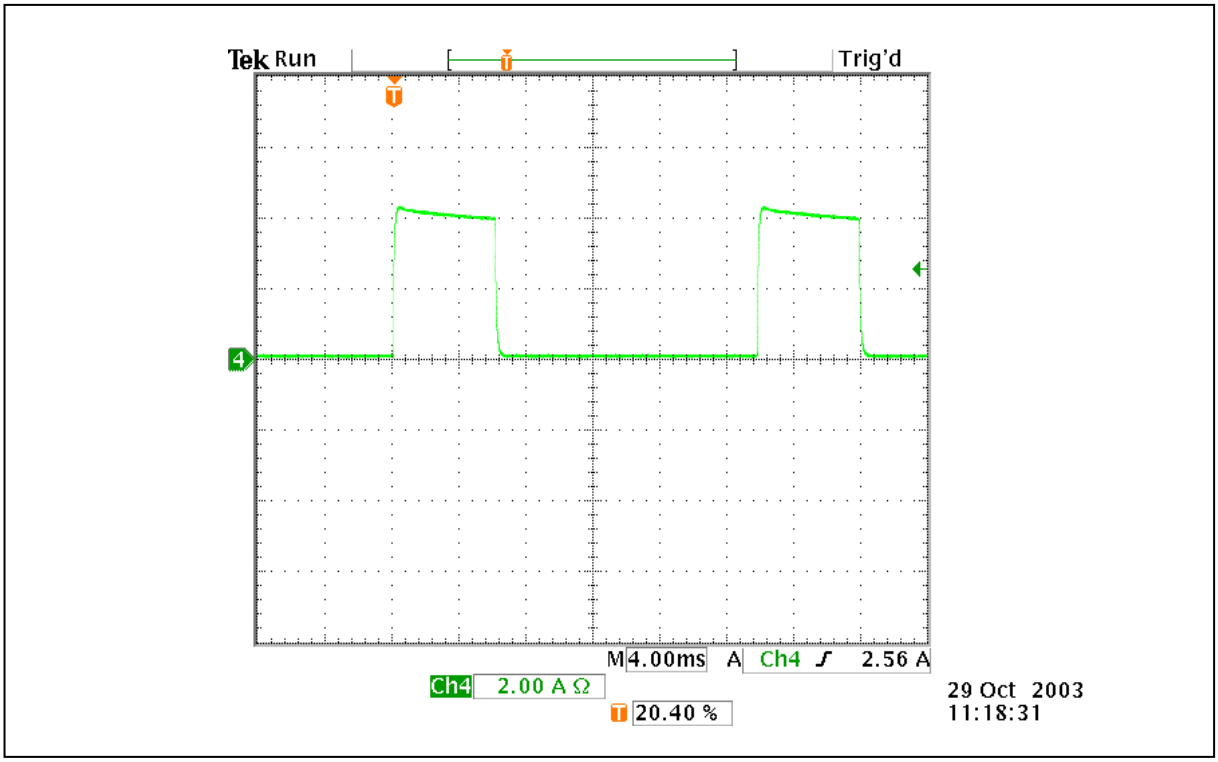
-- Current limit protection: CH1: V_{OUT} CH3: output current



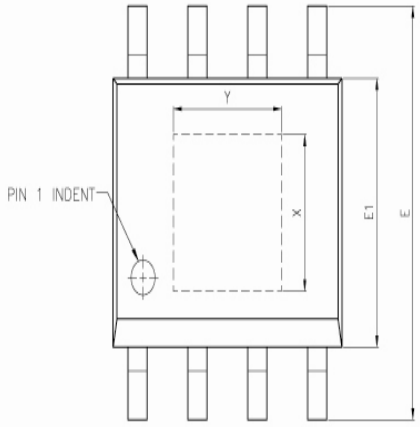
-- Current limit protection (cont.): CH1: V_{OUT}; CH3: output current

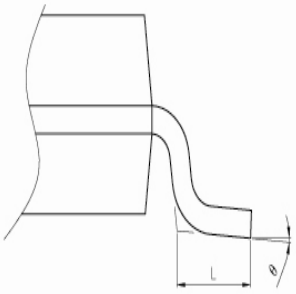


-- Short protection and over temperature protection; CH4: output current

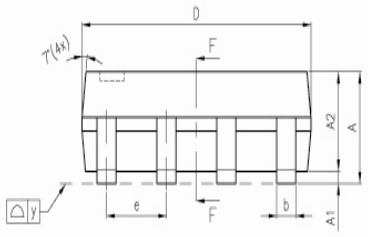


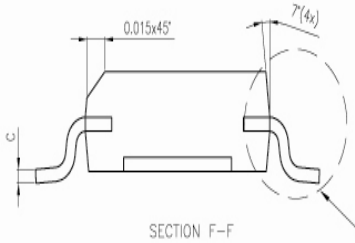
9. PACKAGE DIMENSION (POWER SOP-8)





DETAIL A





SECTION F-F

DETAIL A

NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
⚠ A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

EXPOSED PAD DIMENSION : (MIL)
PAD SIZE: X Y
90*90

10. THERMAL PERFORMANCE

TEST ON FOUR-LAYER (2S2P) JEDEC TEST BOARD							
Package	Power (W)	Component Temp. (°C)					Θ jc (°C /W)
		Package	Die	Downset	Lead	Ambient	
PSOP-8	3.05	100	145	79	78	25	14.7

11. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83310S	8L SOP-8	Commercial, 0°C to +70°C
W83310SG	8L SOP-8(Pb-free package)	Commercial, 0°C to +70°C

12. HOW TO READ THE TOP MARKING

Left line: Winbond logo

1st & 2nd lines: W83310S, **W83310SG (Pb-free package)**

3rd line: Tracking code Tracking code 316 G A

316: Packages assembled in Year 03', week 16

G: assembly house ID; O means OSE, G means GR, etc.

A: The IC version

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.